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December 10, 2001

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Time: 4:15 pm  
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TECHNOLOGY CENTER 2800

TO: Commissioner for Patents  
Attn: Richard A. Booth  
Patent Examining Corps  
Facsimile Center  
Washington, D.C. 20231

FROM: Janal M. Kalis

OUR REF: 303.522US1

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\* Please deliver to Examiner Richard A. Booth in Art Unit 2812. \*

Document(s) Transmitted: A Response Under 1.116 (2 pgs.)

Total pages of this transmission, including cover letter: 3 pgs

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In re. Patent Application of: Alan R. Reinberg

Examiner: Richard A. Booth

Serial No.: 09/382,442

Group Art Unit: 2812

Filed: August 25, 1999

Docket No.: 303.522US1

Title: METHOD FOR REDUCING SINGLE BIT DATA LOSS IN A MEMORY CIRCUIT

Please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

By: Tina M. Pugh

Name: Janal M. Kalis

Reg. No.: Reg. No. 37,650

I hereby certify that this paper is being transmitted by facsimile to the U.S. Patent and Trademark Office on the date shown below.

Tina M. Pugh

12/10/01

Date of Transmission

## EXPEDITED PROCEDURE - EXAMINING GROUP 2812

PATENT# B/Response  
12/10/01  
V. VarnasS/N 09/382,442IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Alan R. Reinberg  
 Serial No.: 09/382,442  
 Filed: August 25, 1999  
 Title: METHOD FOR REDUCING SINGLE BIT DATA LOSS IN A MEMORY CIRCUIT

Examiner: Richard A. Booth  
 Group Art Unit: 2812  
 Docket: 303.522US1

RESPONSE UNDER 37 C.F.R. § 1.116

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REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on October 10, 2001, and the references cited therewith.

No claims are amended, no claims are canceled, and no claims are added; as a result, claims 1-14, 26-32 and 35-39 remain pending in this application.

§103 Rejection of the Claims

Claims 1-14, 26-32, and 35-38 were rejected under 35 USC § 103(a) as being unpatentable over Applicant's admitted prior art in view of Lisenker et al. ((WO 94/19829) or Clark et al. (U.S. Patent No. 5,972,765). The Examiner is maintaining rejection by focusing on the Clark reference which mentions that deuterium provides greater resistance to hot electron stresses than hydrogen. The hot electron stresses referred to are those in MOSFET devices, TFT's, polyresistors and polyemitter bipolars. As has been discussed, none of these references describes a use of deuterium for reducing random single bit data loss in a FLASH memory cell.

The significance of this difference is that FLASH memory includes a programming operation and an erase operation. Both the programming operation and the erase operation must operate in a satisfactory manner for the FLASH memory to perform acceptably. None of the MOSFET devices, TFT's, polyresistors or polyemitter bipolars operate with this two step operation. Thus, there is no precedent in the references cited by the Examiner for concluding that deuterium substitution would work at all to reduce random single bit data loss in a memory cell. The observations described in Lisenker et al. patent suggest that deuterium treatment would